REMARKS

Claims 1-28 are pending in the instant application. Claims 1-28 are rejected. Claims 1, 11 and 20 are amended. No new matter has been added.

103 Rejections

Claims 1-3, 6, 9-13, 16-17, 20-21 and 25-26 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Dye (U.S. Patent No. 6,173,381) in view of Davis et al. (U.S. Patent No. 4,991,169). The Applicant has reviewed the cited references and respectfully submits that the embodiments of the invention as are recited in Claims 1-3, 6, 9-13, 16-17, 20-21 and 25-26 is neither anticipated nor rendered obvious by Dye (U.S. Patent No. 6,173,381) in view of Davis et al.

The Examiner is respectfully directed to independent Claim 1 which sets forth an embodiment of the present invention that includes a controller chip comprising:

> ...an engine operative to manage a memory, the engine including an interface; and a storage element coupled to the engine, the storage element being accessible by a central processing unit (CPU) through the engine, wherein the engine receives commands from the CPU via the interface, manages the storage element via the interface and writes the commands into the memory and wherein the engine incorporates the storage element as part of the memory.

Independent Claims 11 and 20 recite limitations similar to those of Claim 1. Claims 2, 3, 6, 9-10 depend from Claim 1, Claims 12, 13, 16-17 depend from Claim 11, and Claims 21 and 25-26 depend from Claim 20 and set forth further limitations of the claimed invention.

Dye does not anticipate or render obvious a controller chip that includes an engine a memory, and a storage element and features "a storage element coupled to the engine, the storage element being accessible by a central processing unit (CPU) through the engine, wherein the engine receives commands from the CPU via the interface, and manages the storage element via the interface" as is recited in Claim 1 (independent Claims 11 and 20 contain similar limitations). It should be appreciated that in order to meet the aforementioned limitations of Claim 1 the Dye reference must show or suggest an engine that receives commands from a CPU via an interface and manages a storage element via the same interface.

Dye only shows a memory controller that includes embedded data compression and decompression engines and that uses data compression to reduce system bottlenecks. However, the system structure that is disclosed by Dye cannot support the functionality defined in the limitations of Claim 1 cited above (as is discussed below).

Figure 5 of Dye shows an integrated memory controller (IMC) that includes an engine 210 that is coupled to other systems through FIFO buffers 204, 206, 214 and 216. It should be appreciated that engine 210 is coupled to CPU 102 through FIFO buffers 204 and 206 and bus interface logic 202. As Dye discloses at column 13, lines 1-15:

> The bus interface logic 202 couples to an execution engine 210 through two first in first out (FIFO) buffers 204 and 206. In other words, the two FIFO buffers 204 and 206 are coupled between the bus interface logic 202 and the execution engine 210.

It should be noted that because FIFO buffers 204 and 206 are situated between bus interface logic 202 and execution engine 210, execution engine 210 must communicate with (and thus manage) the bus interface logic 202 via FIFO buffers 204 and 206. As such the Dye system is structurally incompatible with a management of FIFO buffers 204 and 206 by execution engine 210 via bus interface logic 202. Consequently, the Applicant respectfully submits that a management of FIFO buffers 204 and 206 by execution engine 210 via bus interface logic 202 cannot be supported by the system disclosed by Dye. This is significant since, as previously discussed, in order to meet the cited limitations of Claim 1 Dye must teach or suggest an engine that receives commands from a CPU via an interface and that manages a storage element via the interface.

It is asserted in the outstanding Office Action (see Office Action page 3), that the recited storage element of Claim 1 is readable on FIFO buffers 204 and 206 (shown in Figure 5) of the Dye reference, and that the recited interface of Claim 1 is readable on bus interface logic 202 (shown in Figure 5) of the Dye reference. It should be noted that the management of a storage element by an engine via an interface from which commands are received from a CPU as recited in Claim 1 is not actually addressed in the Office Action. However, even if a construction of Claim 1 consistent with that actually suggested in the Office Action is employed (e.g., reading its limitations on the aforementioned structures disclosed by Dye as is suggested in the Office Action), the disclosures of Dye are non-the-less insufficient to teach or suggest an embodiment delimited by such, since as outlined above the structure of the Dye system precludes execution engine 210 management of buffers 204 and 206 via bus interface logic 202.

It should be noted that in Dye FIFO buffers 204 and 206 are located adjacent execution engine 210 and are managed directly by execution engine 210. Consequently, although Dye discloses bus interface logic 202, the execution engine 210 does not need to communicate with bus interface logic 202 in order to manage FIFO buffers 204 and 206.

By contrast, the Applicant's disclosed interface is positioned between a graphics engine and a storage element (see Figure 4). In order to manage the storage element commands are transmitted through the disclosed interface. As such, the graphics engine manages the storage element via the interface. Nowhere in the Dye reference is there shown a controller chip engine that receives commands via an interface and manages a storage element via the interface as is set forth in Claims 1, 11 and 20. Consequently, the embodiments of the Applicant's invention as are set forth in Claims 1, 11 and 20 are neither anticipated nor rendered obvious by Dye.

Furthermore, the combination of Davis et al. with Dye does not overcome the deficiencies of Dye in meeting the claim limitations noted above. Davis et al. does not anticipate or render obvious a controller chip that includes an engine, a memory, and a storage element and features "a storage element coupled to the engine, the storage element being accessible by a central processing unit (CPU) through the engine, wherein the engine receives commands from the CPU via the interface, and manages the storage element via the interface" as is recited in Claim 1 (Claims 11 and 20 contain similar limitations). Davis et al. only shows a dual digital signal processor that provides real time links between multiple time division

channels of a digital carrier signal. It should be appreciated that the Davis et al. reference is concerned with providing a system that has the capacity to mediate communications between a carrier and a host system. As a result, nowhere in the Davis et al. reference is there shown a controller chip that includes an engine that receives commands via an interface and manages a storage element via that interface as is set forth in Claim 1 (claims 11 and 20 contain similar limitations). Consequently, the embodiments of the Applicant's invention as are set forth in Claims 1, 11 and 20 are neither anticipated nor rendered obvious by Dye and Davis et al. either alone or in combination.

Therefore, Applicant respectfully submits that Dye and Davis et al. either alone or in combination do not anticipate or render obvious the embodiments of the present claimed invention as are recited in Claims 1, 11 and 20, and as such Claims 1, 11 and 20 are in condition for allowance. Accordingly, Applicant also respectfully submits that Dye and Davis et al. either alone or in combination, do not anticipate or render obvious the embodiments of the present claimed invention as are recited in Claims 2, 3, 6, 9 and 10 dependent on Claim 1, Claims 12, 13 and 16-17 dependent on Claim 11, and Claims 21 and 25-26 dependent on Claim 20, and that Claims 2, 3, 6, 9-10, 12, 13, 16-17, 21 and 25-26 overcomes the basis for rejection under 35 U.S.C. 103(a) as being dependent on allowable base claims.

Claims 4, 5, 7, 8, 14, 15, 18, 19, 22-24, 27 and 28 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Dye (U.S. Patent No. 6,173,381) in view of Davis et al. (U.S. Patent No. 4,991,169) and further in view of an Official Notice. The Applicant has

reviewed the cited references and respectfully submits that embodiments of the present invention as are recited in Claims 4, 5, 7, 8, 14, 15, 18, 19, 22-24, 27 and 28 are neither anticipated nor rendered obvious by Dye (U.S. Patent No. 6,173,381) in view of Davis et al. and further in view of the Official Notice. It should be appreciated that the Official Notice is concerned with the obviousness of utilizing various FIFO buffer geometries but does not address the deficiencies of either Dye or Davis et al. as outlined above. Consequently, the embodiments of the Applicant's invention as set forth in Claims 4, 5, 7, 8, 14, 15, 18, 19, 22-24, 27 and 28 are neither anticipated nor rendered obvious by Dye in view of Davis et al. and further in view of the Official Notice as these Claims are dependent on base Claims 1, 11 and 20 whose allowability are discussed above.

Conclusion

In light of the above-listed remarks, the Applicant respectfully requests allowance of the remaining Claims.

The Examiner is urged to contact the Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,
WAGNER, MURABITO & HAO LLP

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Reginald A. Ratliff
Registration No. 48,098
Two North Market Street
Third Floor
San Jose, CA 95113
(408) 938-9060